IN THE MATTER OF
Patent Application

CERTIFICATE

I, Yukari NAKAMOTO, residing at 3-13-201, Higashinara 1-chome, Ibaraki-shi, Osaka, Japan, hereby declare that the document attached hereto is a translation made by me of the Japanese Patent Application number **2003-056860** and certify that it is a true translation to the best of my knowledge and belief.

Dated this **27th** day of **September, 2005**

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Yukari NAKAMOTO

[Name of the Document] Specification

[Title of the Invention] SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR

[Claims]

[Claim 1] A fabrication method for a semiconductor device, characterized by comprising the steps of:

(a) forming a gate electrode on a semiconductor region of a first conductivity type with a gate insulating film interposed therebetween;

(b) forming extension implanted layers in the semiconductor region by implanting first impurities of a second conductivity type in the semiconductor region using the gate electrode as a mask;

(c) after the step (b), forming fluorine implanted layers in the semiconductor region by implanting fluorine in the semiconductor region using the gate electrode as a mask; and

(d) after the step (c), forming high-density extension diffused layers of the second conductivity type made from diffusion of the first impurities by performing first heat treatment on the semiconductor region.

[Claim 2] The semiconductor device fabrication method of Claim 1, characterized in that the dose of fluorine in the step (c) is not less than $1 \times 10^{13}/cm^2$ and also in the level at which the semiconductor region is kept from becoming amorphous.

[Claim 3] The semiconductor device fabrication method of Claim 2, characterized in that the dose of fluorine in the step (c) is less than $3 \times 10^{14}/cm^2$.

[Claim 4] The semiconductor device fabrication method of any one of Claims 1 to 3, characterized in that the implantation projected range of fluorine in the step (c) is roughly the same as the implantation projected range of the first impurities in the step (b).

[Claim 5] The semiconductor device fabrication method of any one of Claims 1 to

4, characterized in that the step (b) includes the step of forming pocket implanted layers in the semiconductor region by implanting second impurities of the first conductivity type in the semiconductor region using the gate electrode as a mask, and

in the step (d), pocket diffused layers of the first conductivity type made from diffusion of the second impurities are formed to be in contact with and under the high-density extension diffused layers by performing the first heat treatment.

[Claim 6] The semiconductor device fabrication method of any one of Claims 1 to 5, characterized in that after the step (d), the method further comprises the steps of:

(e) forming sidewalls made of an insulating film on walls of the gate electrode;

(f) forming high-density source/drain implanted layers in the semiconductor region by implanting third impurities of the second conductivity type in the semiconductor region using the gate electrode and the sidewalls as a mask; and

(g) after the step (f), forming high-density source/drain diffused layers of the second conductivity type made from diffusion of the third impurities below the outer side of the sidewall by performing second heat treatment on the semiconductor region.

[Claim 7] The semiconductor device fabrication method of any one of Claims 1 to 6, characterized in that in the step (d), the fluorine in the fluorine implanted layers diffuses while interacting with point defects, so that excessive point defects induced in the semiconductor region are removed.

[Claim 8] The semiconductor device fabrication method of any one of Claims 1 to 7, characterized by further comprising the step of:

performing extremely low temperature heat treatment before the step (d) and after the step (c), to recover only crystal damage produced in the semiconductor region due to the implantation of the first impurities and the fluorine without substantially allowing diffusion of the first impurities in the extension implanted layers.

[Claim 9] The semiconductor device fabrication method of Claim 8, characterized in that the extremely low temperature heat treatment has a heating temperature of 400° C to 600° C.

[Claim 10] The semiconductor device fabrication method of any one of Claims 1 to 9, characterized in that the first heat treatment in the step (d) is rapid thermal annealing in which the temperature rise rate is about 100° C/s or more, the temperature drop rate is about 80° C/s or more, the heating temperature is about 850° C to 1050° C, and the peak temperature is held for about ten seconds at the longest or is not held at all.

[Claim 11] The semiconductor device fabrication method of any one of Claims 1 to 10, characterized in that the first impurities in the step (b) are boron, boron fluoride or indium.

[Claim 12] The semiconductor device fabrication method of any one of Claims 1 to 10, characterized in that the first impurities in the step (b) are arsenic.

[Claim 13] The semiconductor device fabrication method of Claim 12, characterized in that during the first heat treatment in the step (d), the first impurities in the extension implanted layers diffuse in a state in which the fluorine has captured atomic vacancies produced in top portions of the semiconductor region.

[Claim 14] The semiconductor device fabrication method of any one of Claims 1 to 13, characterized in that the dose for the implantation of the first impurities in the step (b) is in a level at which the semiconductor region is kept from becoming amorphous, and

the high-density extension diffused layers having a predetermined impurity concentration are formed by repeating a series of process steps composed of implanting the first impurities in the step (b), implanting fluorine in the step (c) and performing the first heat treatment in the step (d).

[Claim 15] A semiconductor device, characterized by comprising:

a gate electrode formed on a semiconductor region of a first conductivity type with a gate insulating film interposed therebetween; and

high-density extension diffused layers of a second conductivity type formed in portions of the semiconductor region on the sides of the gate electrode,

wherein the high-density extension diffused layers are crystal layers that contain fluorine and are free from residual defects.

[Detailed Description of the Invention]

[Field of the Invention]

The present invention relates to a semiconductor device and a fabrication method for the same. In particular, the present invention relates to a semiconductor device that can be made finer, has shallow-junction, low-resistance diffused layers and also can operate at high speed, and a fabrication method for such a semiconductor device.

[Prior Art]

With the tendency of higher integration of semiconductor integrated circuits, finer MIS transistors have been demanded. To respond to this demand, MIS transistors having shallow-junction, low-resistance, high-density extension diffused layers are required.

A conventional fabrication method for a semiconductor device will be described with reference to the drawings (see patent literature 1).

FIGS. **9(a)** to **9(e)** are cross-sectional views for illustrating process steps of a conventional fabrication method for a semiconductor device.

In the step shown in FIG. **9(a)**, arsenic (As) ions and phosphorus (P) ions as n-type impurities are implanted in a p-type semiconductor substrate **200**. The resultant substrate is subjected to heat treatment, to form an n-type channel diffused layer **203** containing arsenic impurities in the top portion of the semiconductor substrate **200** and an n-type well layer **204** containing phosphorus impurities in a portion under the n-type channel diffused

layer **203**.

In the step shown in FIG. **9(b)**, a silicon oxide film and a polysilicon film are sequentially formed on the resultant semiconductor substrate **200**, and then patterned by photolithography and dry etching, to form a gate oxide film **201** and a gate electrode **202**.

In the step shown in FIG. **9(c)**, As ions as n-type impurities are implanted in the semiconductor substrate **200** using the gate electrode **202** as a mask, to form n-type pocket implanted layers **207A**. Subsequently, boron (B) as p-type impurities are implanted in the semiconductor substrate **200** using the gate electrode **202** as a mask, to form p-type extension implanted layers **206A**.

In the step shown in FIG. **9(d)**, a silicon nitride film is deposited over the entire top surface of the semiconductor substrate **200** and then etched by anisotropic etching, to form sidewalls **208** on the walls of the gate electrode **202**.

In the step shown in FIG. **9(e)**, BF_2 ions as p-type impurities are implanted in the semiconductor substrate **200** using the gate electrode **202** and the sidewalls **208** as a mask, to form high-density source/drain implanted layers. The resultant substrate is subjected to high-temperature, short-time heat treatment, to form p-type high-density source/drain diffused layers **205**, p-type extension diffused layers **206** and n-type pocket diffused layers **207**.

[Patent Literature]

Japanese Laid-Open Patent Publication No. 2002-76136

[Problems that the Invention is to solve]

In the conventional fabrication method for a semiconductor device, the boron implantation energy for formation of the p-type extension implanted layers **206A** tends to be made low in the process of forming the p-type extension diffused layers **206**, to thereby attain a shallow junction.

However, even in a structure in which boron is implanted in the semiconductor substrate **200** under low-energy, high-dose implantation conditions so as to form the p-type extension implanted layers **206A** having a shallow junction, there arises a problem as follows. Subsequent high-temperature, short-time heat treatment causes transient enhanced diffusion (hereinafter, referred to as TED) of boron and thus boron is diffused deep into a region, resulting in failure to form the p-type extension diffused layers **206** having a desired impurity profile. The TED as used herein refers to an abnormal diffusion phenomenon in which impurity atoms interact with excessive point defects (such as interstitial silicon atoms and atomic vacancies) existing in the semiconductor substrate, resulting in enhancement of diffusion of the impurity atoms. The excessive point defects are mainly introduced by implantation damage occurring during ion implantation in many cases.

Hence, in the conventional fabrication method for a semiconductor device described above, even though the ion implantation energy is lowered to attain a shallower junction, the TED of implanted dopants increases. Therefore, it is difficult to form MIS transistors having shallow-junction, low-resistance extension diffused layers only by implanting ions of a single element at a low energy.

An object of the present invention is providing a semiconductor device having high-density extension diffused layers having a shallow junction and low resistance, and a fabrication method for such a semiconductor device.

[Means for Solving the Problems]

To attain the above object, in the fabrication method for a semiconductor device of the present invention, fluorine is implanted immediately after impurities for formation of extension diffused layers are implanted, to allow the implanted fluorine to react with interstitial silicon atoms that may enhance diffusion of the implanted impurities. This

reduces the number of such interstitial silicon atoms, and in this way, shallow-junction, low-resistance, high-density extension diffused layers can be formed.

Specifically, the semiconductor device fabrication method for a semiconductor device of the present invention includes the steps of: (a) forming a gate electrode on a semiconductor region of a first conductivity type with a gate insulating film interposed therebetween; (b) forming extension implanted layers in the semiconductor region by implanting first impurities of a second conductivity type in the semiconductor region using the gate electrode as a mask; (c) after the step (b), forming fluorine implanted layers in the semiconductor region by implanting fluorine in the semiconductor region using the gate electrode as a mask; and (d) after the step (c), forming high-density extension diffused layers of the second conductivity type made from diffusion of the first impurities by performing first heat treatment on the semiconductor region.

That is, extension implanted layers are first formed by implanting first impurities using the gate electrode formed on the semiconductor region via the gate insulating film as a mask. Fluorine implanted layers are then formed by implanting fluorine.. Thereafter, first heat treatment is performed for activating the first impurities in the extension implanted layers.

With this structure, fluorine in the fluorine implanted layers rapidly diffuse while reacting with point defects that may cause transient enhanced diffusion of impurities during first heat treatment. This reduces the number of excessive point defects that are supposed to interact with the impurities, and thus suppresses the transient enhanced diffusion of the impurities. As a result, shallow, low-resistance extension diffused layers can be formed. In addition, when the impurity element is boron, implanted boron ions are known to react with interstitial silicon atoms to produce boron-interstitial silicon clusters and be inactivated. By the reduction of the number of excessive point defects, the

production of boron-interstitial silicon clusters is suppressed. Thus, this inactivation of boron can also be suppressed. Accordingly, shallow, low-resistance, high-density extension diffused layers are formed.

In the fabrication method for a semiconductor device described above, the dose of fluorine in the step (c) is not less than $1 \times 10^{13}/cm^2$ and also in a level at which the semiconductor region is kept from becoming amorphous. In this case, the dose of fluorine in the step (c) is preferably less than $3 \times 10^{14}/cm^2$.

In the semiconductor device fabrication method, the implantation projected range of fluorine in the step (c) is preferably roughly the same as the implantation projected range of the first impurities in the step (b).

In the semiconductor device fabrication method, the step (b) includes the step of forming pocket implanted layers in the semiconductor region by implanting second impurities of the first conductivity type in the semiconductor region using the gate electrode as a mask, and in the step (d), pocket diffused layers of the first conductivity type made from diffusion of the second impurities are formed to be in contact with portions of the semiconductor region under the high-density extension diffused layer by performing the first heat treatment.

The semiconductor device fabrication method further includes, after the step (d), the steps of: (e) forming sidewalls made of an insulating film on walls of the gate electrode; (f) forming high-density source/drain implanted layers in the semiconductor region by implanting third impurities of the second conductivity type in the semiconductor region using the gate electrode and the sidewalls as a mask; and (g) after the step (f), forming high-density source/drain diffused layers of the second conductivity type made from diffusion of the third impurities below the outer side of the sidewall.

In the semiconductor device fabrication method, in the step (d), the fluorine in the

fluorine implanted layers diffuses while interacting with point defects, so that excessive point defects induced in the semiconductor region are removed.

The semiconductor device fabrication method further includes the step of: performing extremely low temperature heat treatment before the step (d) and after the step (c), to recover only crystal damage produced in the semiconductor region due to the implantation of the first impurities and the fluorine without substantially allowing diffusion of the first impurities in the extension implanted layer.

In the semiconductor device fabrication method, the extremely low temperature heat treatment has a heating temperature of 400° C to 600° C.

In the semiconductor device fabrication method, the first heat treatment in the step (d) is rapid thermal annealing in which the temperature rise rate is about 100° C/s or more, the temperature drop rate is about 80° C/s or more, the heating temperature is about 850° C to 1050° C, and the peak temperature is held for about ten seconds at the longest or is not held at all.

In the semiconductor device fabrication method, the first impurities in the step (b) are boron, boron fluoride or indium.

In the semiconductor device fabrication method, the first impurities in the step (b) are arsenic.

In the semiconductor device fabrication method, during the first heat treatment in the step (d), the first impurities in the extension implanted layers diffuse in a state in which the fluorine has captured atomic vacancies produced in top portions of the semiconductor region.

In the semiconductor device fabrication method, the dose for the implantation of the first impurities in the step (b) is in a level at which the semiconductor region is kept from becoming amorphous, and the high-density extension diffused layers having a

predetermined impurity concentration are formed by repeating a series of process steps composed of implanting the first impurities in the step (b), implanting fluorine in the step (c) and performing the first heat treatment in the step (d).

The semiconductor device of the present invention includes: a gate electrode formed on a semiconductor region of a first conductivity type with a gate insulating film formed therebetween; and high-density extension diffused layers of a second conductivity type formed in portions of the semiconductor region on the sides of the gate electrode, wherein the high-density extension diffused layers are crystal layers that contain fluorine and are free from residual defects.

[Embodiments of the Invention]

(Embodiment 1)

Embodiment 1 of the present invention will be described with reference to the accompanying drawings.

FIGS. **1(a)** to **1(d)** and **2(a)** to **2(d)** are cross-sectional views for illustrating process steps of a fabrication method for a semiconductor device of Embodiment 1 of the present invention.

First, in a process step shown in FIG. **1(a)**, arsenic (As) ions as n-type impurities are implanted in a channel formation region of a semiconductor substrate **100** made of p-type silicon under the conditions of an implantation energy of 140 keV and an implantation dose of $5 \times 10^{12}/cm^2$, to form an n-type channel implanted layer **103A**. Subsequently, phosphorus (P) ions as n-type impurities are implanted in an n-type well formation region of the semiconductor substrate **100** twice, first under the first implantation conditions of an implantation energy of 260 keV and an implantation dose of $1 \times 10^{12}/cm^2$ and then under the second implantation conditions of an implantation energy of 540 keV and an implantation dose of $1 \times 10^{13}/cm^2$, to form an n-type well implanted layer (not shown).

In a process step shown in FIG. **1(b)**, immediately after formation of the n-type channel implanted layer **103A** and the n-type well implanted layer, the semiconductor substrate **100** is subjected to first rapid thermal annealing (RTA) in which the temperature of the semiconductor substrate **100** is raised to about 850° C to about 1050° C at a rise rate of about 100° C/s or more, preferably about 200° C/s, and then the peak temperature is held for ten seconds at the longest or is not held at all. With this first thermal annealing, an n-type channel diffused layer **103**, made from diffusion of the arsenic ions implanted in the n-type channel implanted layer **103A**, is formed in the surface portion of the semiconductor substrate **100**. Simultaneously, an n-type well diffused layer **104**, made from diffusion of the phosphorus ions implanted in the n-type well implanted layer, is formed in a portion under the n-type channel diffused layer **103** to be in contact with the n-type channel diffused layer **103**. Note herein that the rapid thermal annealing involving no holding of the peak temperature refers to a kind of heat treatment in which the heat treatment temperature is lowered as soon as it reaches the peak.

In a process step shown in FIG. **1(c)**, a silicon oxide film having a thickness of about 1.5 nm and a polysilicon film having a thickness of about 150 nm are formed in this order over the semiconductor substrate **100**. The silicon oxide film and the polysilicon film are then patterned by photolithography and dry etching, to form a gate insulating film **101** and a gate electrode **102**, respectively. In place of the silicon oxide film, a silicon oxide nitride (SiON) film or a high dielectric insulating film (high-k film) such as a hafnium oxide (HfO_x) film may be used as the gate insulating film. In place of the polysilicon film, a polymetal film may be used as the gate electrode.

In a process step shown in FIG. **1(d)**, boron (B) ions as p-type impurities are implanted in the semiconductor substrate **100** using the gate electrode **102** as a mask under the conditions of an implantation energy of 1 keV and an implantation dose of $3 \times 10^{14}/cm^2$,

to form p-type extension implanted layers **106A**. In this process step, arsenic (As) ions as n-type impurities are implanted in the semiconductor substrate **100** using the gate electrode **102** as a mask under the conditions of an implantation energy of 130 keV and an implantation dose of $4 \times 10^{13}/cm^2$, to form n-type pocket impurity implanted layers **107A** in regions of the semiconductor substrate **100** under the p-type extension implanted layers **106A**. The p-type extension implanted layers **106A** and the n-type pocket impurity implanted layers **107A** are preferably shallower than the n-type channel diffused layer **103**.

In a process step shown in FIG. **2(a)**, fluorine ions are then implanted in the semiconductor substrate **100** using the gate electrode **102** as a mask under the conditions of an implantation energy of 2 keV and an implantation dose of $5 \times 10^{13}/cm^2$, to form fluorine implanted layers **109**. The fluorine dose in this implantation should be not less than $1 \times 10^{13}/cm^2$ and also in the level at which the semiconductor substrate is kept from becoming amorphous, preferably, less than $3 \times 10^{14}/cm^2$. The implantation projected range of fluorine should be less than five times as large as the range of boron in the formation of the extension implanted layers, preferably roughly the same as the range of boron.

In a process step shown in FIG. **2(b)**, the resultant semiconductor substrate **100** is subjected to second rapid thermal annealing in which the temperature of the semiconductor substrate **100** is raised to about 850° C to about 1050° C at a rise rate of about 100° C/s or more, preferably about 200° C/s, then the peak temperature is held for ten seconds at the longest or is not held at all, and the temperature is lowered at a drop rate of about 80° C/s. With the second rapid thermal annealing, p-type high-density extension diffused layers **106** having a shallow junction, made from diffusion of the boron ions contained in the p-type extension implanted layers **106A**, are formed in regions of the semiconductor substrate **100** on both sides of the gate electrode **102**. Simultaneously, n-type pocket diffused layers **107**, made from diffusion of the arsenic ions contained in the n-type pocket

implanted layers **107A**, are formed in regions under the p-type high-density extension diffused layers **106** to be in contact with the extension diffused layers **106**.

In a process step shown in FIG. **2(c)**, a silicon nitride film having a thickness of about 50 nm is deposited over the entire top surface of the semiconductor substrate **100** including the gate electrode **102** by CVD, for example. The deposited silicon nitride film is then subjected to anisotropy etching, to form sidewalls **108** made of the silicon nitride film on both walls of the gate electrode **102**. In place of the silicon nitride film, a silicon oxide film or a silicon oxide nitride film may be used as the sidewalls **108**. Otherwise, a laminate film composed of at least two films among a silicon nitride film, a silicon oxide film and a silicon oxide nitride film may be used.

In a process step shown in FIG. **2(d)**, boron as p-type impurities are implanted in the semiconductor substrate **100** using the gate electrode **102** and the sidewalls **108** as a mask under the conditions of an implantation energy of 10 and an implantation dose of $3 \times 10^{15}/cm^2$. The resultant semiconductor substrate **100** is subjected to third rapid thermal annealing in which the temperature of the semiconductor substrate **100** is raised to about 850° C to about 1050° C at a rise rate of about 200° C/s to 250° C/s, and then the peak temperature is held for ten seconds at the longest or is not held at all. With the third rapid thermal annealing, p-type high-density source/drain diffused layers **105**, made from diffusion of the boron ions in the high-density source/drain implanted layers, are formed in regions of the semiconductor substrate **100** on both outer sides of the sidewalls **108**. The p-type high-density source/drain diffused layers **105** have a junction deeper than the n-type pocket diffused layers **107**. As a result, the p-type high-density extension diffused layers **106** and the n-type pocket diffused layers **107** exist only under the sidewalls **108**.

In the fabrication method for a semiconductor device of Embodiment 1, boron ion implantation for formation of the p-type extension implanted layers **106A** is performed at a

low energy, and then ion implantation for the fluorine implanted layers **109** is performed at a dose low enough to keep the semiconductor substrate from becoming amorphous. Thereafter, the boron ions in the p-type extension implanted layers **106A** are activated by the second rapid thermal annealing.

The inventors of the present invention examined an influence of fluorine on boron diffusion. As a result of this examination, the inventors have found that there are optimum fluorine implantation conditions for suppressing TED of boron. This will be described with reference to FIG. **3**.

FIG. **3(a)** is a graph showing variations of the change of the junction depth of boron with the annealing time. In this graph, the solid curve shows change of the junction depth observed when only boron implantation is performed with no implantation of fluorine and then heat treatment is performed. The broken line represents the change of the junction depth observed when fluorine is implanted at a dose high enough to allow the substrate to become amorphous and then heat treatment is performed. The one-dot chain line represents the change of the junction depth observed when fluorine is implanted at a dose low enough to keep the substrate from becoming amorphous and then heat treatment is performed.

As is found from FIG. **3(a)**, in the case in which fluorine is implanted at a dose low enough to keep the substrate from becoming amorphous, diffusion of boron is suppressed, compared with the case of implanting no fluorine. In the case of implanting fluorine at a dose high enough to allow the substrate to become amorphous, however, boron diffuses more deeply than in the case of implanting no fluorine. Accordingly, a feature of the present invention is implanting fluorine under a condition with which diffusion of the boron can be suppressed, that is, at a dose with which the semiconductor substrate is kept from becoming amorphous. By implanting fluorine under this condition, the TED of boron

is suppressed during the heat treatment for formation of the p-type high-density extension diffused layers **106**, and thus the junction depth does not extend deeply. Accordingly, the p-type high-density extension diffused layers **106** having a shallow junction can be formed. In addition, since diffusion of the boron toward the surface of the semiconductor substrate is also suppressed, the boron dose loss is suppressed. Thus, the p-type high-density extension diffused layers **106** having low resistance can be attained.

FIG. **3(b)** shows variations of the boron areal density in the semiconductor substrate with the annealing time. In FIG. **3(b)**, the solid line represents the case of implanting no fluorine. The broken line represents the case of implanting fluorine at a high dose. The one-dot chain line represents the case in which fluorine is implanted at a low dose and then heat treatment is performed.

As is found from FIG. **3(b)**, the boron dose loss increases when fluorine is implanted in the substrate. The increase of the boron dose loss can be suppressed by decreasing the dose of fluorine to as low as $1 \times 10^{14}/cm^2$ or less, for example. Accordingly, the boron dose loss that occurs during the annealing can be suppressed. Thus, the extension diffused layers having low resistance and a shallow junction can be formed without the necessity of unnecessarily increasing the dose for the extension implanted layers.

The fluorine in the fluorine implanted layers rapidly diffuses toward the silicon surface and comes out of the substrate during the heat treatment. Therefore, the implantation projected range of fluorine should preferably be roughly equal to or a little deeper than the range of boron.

The fluorine implantation is performed after the formation of the extension implanted layers by low-energy boron implantation. Therefore, the impurity profile of boron is free from influence of the fluorine implantation, and this permits design of the

impurity profile.

In place of implanting boron and fluorine separately as described above, BF_2 implantation may be used to give simultaneous implantation of boron and fluorine. However, in use of BF_2 implantation, fluorine will be invariably implanted at a dose twice as high as the dose of boron. Therefore, if BF_2 is implanted at a high dose to allow formation of the extension diffused layers, high-concentration fluorine is implanted. This will make the semiconductor substrate amorphous, and as a result, the effect of suppressing boron diffusion will not be obtained.

In consideration of the above, fluorine is implanted under the implantation condition described above so that TED-induced abnormal diffusion of boron can be suppressed. This ensures formation of MIS transistors including the low-resistance, high-density extension diffused layers **106** in which the impurity profile is steep, the junction is shallow, and increase in resistance value due to dose loss is suppressed. Thus, a semiconductor device including fine MIS transistors having high driving force can be formed.

Moreover, the high-density source/drain diffused layers **105** of the resultant MIS transistor contain fluorine and are made of a crystal layer including no residual defect layer such as an end of range (EOR) defect. This can reduce occurrence of junction leakage caused by such a residual defect layer. The EOR defect as used herein refers to a defect layer that may be produced in the vicinity of the position (in the depth) of an amorphous-crystal interface formed immediately after ion implantation if the semiconductor substrate is subjected to heat treatment in an amorphous state.

Accordingly, a semiconductor device including fine MIS transistors having high driving force and reduced junction leakage can be provided.

(Embodiment 2)

Embodiment 2 of the present invention will be described with reference to the drawings.

FIGS. **4(a)** to **4(e)** and **5(a)** to **5(d)** are cross-sectional views for illustrating process steps of a fabrication method for a semiconductor device of Embodiment 2 of the present invention.

First, as shown in FIG. **4(a)**, arsenic (As) ions as n-type impurities are implanted in a channel formation region of a semiconductor substrate **100** made of p-type silicon under the conditions of an implantation energy of 140 keV and an implantation dose of $5 \times 10^{12}/cm^2$, to form an n-type channel implanted layer **103A**. Subsequently, phosphorus (P) ions as n-type impurities are implanted in an n-type well formation region of the semiconductor substrate **100** twice, first under the first implantation conditions of an implantation energy of 260 keV and an implantation dose of $1 \times 10^{12}/cm^2$ and then under the second implantation conditions of an implantation energy of 540 keV and an implantation dose of $1 \times 10^{13}/cm^2$, to form an n-type well implanted layer (not shown).

As shown in FIG. **4(b)**, immediately after formation of the n-type channel implanted layer **103A** and the n-type well implanted layer, the semiconductor substrate **100** is subjected to first rapid thermal annealing (RTA) in which the temperature of the semiconductor substrate **100** is raised to about 850° C to about 1050° C at a rise rate of about 100° C/s or more, preferably about 200° C/s, and then the peak temperature is held for ten seconds at the longest or is not held at all. With the first rapid thermal annealing, an n-type channel diffused layer **103**, made from diffusion of the arsenic ions implanted in the n-type channel implanted layer **103A**, is formed in the surface portion of the semiconductor substrate **100**. Simultaneously, an n-type well diffused layer **104**, made from diffusion of the phosphorus ions implanted in the n-type well implanted layer is formed in a portion under the n-type channel diffused layer **103** to be in contact with the n-

type channel diffused layer **103**. Note herein that the rapid thermal annealing involving no holding of the peak temperature refers to a kind of heat treatment in which the heat treatment temperature is lowered as soon as it reaches the peak.

As shown in FIG. **4(c)**, a silicon oxide film having a thickness of about 1.5 nm and a polysilicon film having a thickness of about 150 nm are formed in this order over the semiconductor substrate **100**. The silicon oxide film and the polysilicon film are then patterned by photolithography and dry etching, to form a gate insulating film **101** and a gate electrode **102**, respectively. In place of the silicon oxide film, a silicon oxide nitride (SiON) film or a high dielectric insulating film (high-k film) such as a hafnium oxide (HfO_x) film may be used as the gate insulating film **101**. In place of the polysilicon film, a polymetal film may be used as the gate electrode.

As shown in FIG. **4(d)**, arsenic (As) ions as n-type impurities are implanted in the semiconductor substrate **100** using the gate electrode **102** as a mask under the conditions of an implantation energy of 130 keV and an implantation dose of $4 \times 10^{13}/cm^2$, to form n-type pocket impurity implanted layers **107A**. Subsequently, boron (B) ions as p-type impurities are implanted in the semiconductor substrate **100** using the gate electrode **102** as a mask under the conditions of an implantation energy of 1 keV and an implantation dose of $3 \times 10^{14}/cm^2$, to form p-type extension implanted layers **106A** having an implantation depth shallower than the n-type pocket impurity implanted layers **107A**. The p-type extension implanted layers **106A** and the n-type pocket impurity implanted layers **107A** are preferably shallower than the n-type channel diffused layer **103**.

As shown in FIG. **4(e)**, fluorine ions are implanted in the semiconductor substrate **100** using the gate electrode **102** as a mask under the conditions of an implantation energy of 2 keV and an implantation dose of $5 \times 10^{13}/cm^2$, to form fluorine implanted layers **109**. The fluorine dose in this implantation should be not less than $1 \times 10^{13}/cm^2$ and also in the

level at which the semiconductor substrate is kept from becoming amorphous, preferably, less than $3 \times 10^{14}/cm^2$. The implantation projected range of fluorine should be less than five times as large as the range of boron in the formation of the p-type extension implanted layers, preferably roughly the same as the range of boron.

As shown in FIG. **5(a)**, immediately after formation of the p-type extension implanted layers **106A**, the n-type pocket impurity implanted layers **107A** and the fluorine implanted layers **109** by ion implantation, the semiconductor substrate **100** is subjected to extremely low temperature heat treatment in which the temperature of the semiconductor substrate **100** is raised to about 400° C to about 600° C and held for about ten hours at the largest. By this extremely low temperature heat treatment, the impurities in p-type extension implanted annealed layers **106B** and n-type pocket implanted annealed layers **107B** are hardly diffused but only crystal damage produced during the ion implantation is recovered.

As shown in FIG. **5(b)**, the resultant semiconductor substrate **100** is subjected to second rapid thermal annealing in which the temperature of the semiconductor substrate **100** is raised to about 850° C to about 1050° C at a rise rate of about 100° C/s or more, preferably about 200° C/s, then the peak temperature is held for ten seconds at the longest or is not held at all, and the temperature is lowered at a drop rate of about 80° C/s. With the second rapid thermal annealing, p-type high-density extension diffused layers **106** having a shallow junction, made from diffusion of the boron ions contained in the p-type extension implanted annealed layers **106B**, are formed in regions of the semiconductor substrate **100** on both sides of the gate electrode **102**. Simultaneously, n-type pocket diffused layers **107**, made from diffusion of the arsenic ions contained in the n-type pocket implanted annealed layers **107B**, are formed in regions under the extension diffused layers **106** to be in contact with the extension diffused layers **106**.

As shown in FIG. **5(c)**, a silicon nitride film having a thickness of about 50 nm is deposited over the entire top surface of the semiconductor substrate **100** including the gate electrode **102** by CVD, for example. The deposited silicon nitride film is then subjected to anisotropy etching, to form sidewalls **108** made of the silicon nitride film on both walls of the gate electrode **102**. In place of the silicon nitride film, a silicon oxide film or a silicon oxide nitride film may be used as the sidewalls **108**. Otherwise, a laminate film composed of at least two films among a silicon nitride film, a silicon oxide film and a silicon oxide nitride film may be used.

As shown in FIG. **5(d)**, boron as p-type impurities are implanted in the semiconductor substrate **100** using the gate electrode **102** and the sidewalls **108** as a mask under the conditions of an implantation energy of 10 keV and an implantation dose of $3 \times 10^{15}/cm^2$, to form high-density source/drain implanted layers. The resultant semiconductor substrate **100** is subjected to third rapid thermal annealing in which the temperature of the semiconductor substrate **100** is raised to about 850° C to about 1050° C at a rise rate of about 200° C/s to 250° C/s, and then the peak temperature is held for ten seconds at the longest or is not held at all. With the third rapid thermal annealing, p-type high-density source/drain diffused layers **105**, made from diffusion of the boron ions in the high-density source/drain implanted layers, are formed in regions of the semiconductor substrate **100** on both outer sides of the sidewalls **108**. The p-type high-density source/drain diffused layers **105** are connected with the p-type high-density extension diffused layers **106** and have a junction deeper than the p-type high-density extension diffused layers **106**. The junction of the p-type high-density source/drain diffused layers **105** should also be deeper than the junction of the n-type pocket diffused layers **107**. As a result, the p-type high-density extension diffused layers **106** and the n-type pocket diffused layers **107** exist only under the sidewalls **108**.

FIG. **6** show impurity profiles in the depth direction from the substrate surface in some steps of the fabrication method for a semiconductor device of Embodiment 2. FIG. **6A** shows the impurity profiles observed immediately after the ion implantation, in which the solid line represents the boron distribution immediately after formation of the p-type extension implanted layers **106A** shown in FIG. **4(d)**, and the broken line represents the fluorine distribution immediately after formation of the fluorine implanted layers **109** shown in FIG. **4(e)**. FIG. **6(b)** shows the impurity profiles observed immediately after the extremely low temperature heat treatment, in which the solid line represents the boron distribution in the p-type extension implanted annealed layers **106B** in FIG. **5(a)**, and the broken line represents the fluorine distribution in the fluorine implanted annealed layers **109B** in FIG. **5(a)**. FIG. **6(c)** shows the impurity profiles observed after the activation heat treatment, in which the solid line represents the boron distribution in the p-type high-density extension diffused layers **106** in FIG. **5(b)**.

A feature of this embodiment is that the extremely low temperature heat treatment at a temperature of about 400° C to about 600° C is performed in the step shown in FIG. **5(a)** after the implantation, to recover crystal damage layers produced in the respective steps of ion implantation. The extremely low temperature range, which is a range of the order of 400° C, is a temperature range in which a solid-phase regrowth phenomenon known as solid-phase epitaxial regrowth occurs when the substrate is amorphous. As is found from FIGS. **6(a)** and **6(b)**, the impurity profiles after the extremely low temperature heat treatment, in comparison with the impurity profiles immediately after the ion implantation, dopants normally used are hardly diffused because the diffusion coefficients of such dopants are sufficiently small compared with the diffusion coefficients of point defects. However, in the fluorine implanted layers **109**, fluorine diffuses rapidly even in the extremely low temperature range of about 400° C. Hence, by performing heat

treatment in this extremely low temperature range, point defects and fluorine can be selectively diffused. In other words, fluorine diffuses while interacting with point defects. In this way, most of excessive point defects produced during the ion implantation can be eliminated during the extremely low temperature heat treatment. Moreover, the position of the junction of the p-type extension implanted annealed layers **106B** little changes by the extremely low temperature heat treatment from the position observed immediately after the ion implantation.

The extremely low temperature heat treatment only is insufficient for activation of the implanted impurities. Therefore, immediately after the extremely low temperature heat treatment, rapid thermal annealing (such as spike RTA and flash lamp annealing) is performed in the step shown in FIG. **5(b)**, to activate the impurities. The rapid thermal annealing is performed after the sufficient elimination of excessive point defects by the extremely low temperature heat treatment. Hence, TED-induced abnormal diffusion of impurities can be suppressed as shown in FIG. **6(c)**. As a result, activation of impurities can be attained while the steep impurity profile and the shallow junction are maintained.

In the fabrication method for a semiconductor device of Embodiment 2, ion implantation for formation of the p-type extension implanted layers **106A** is performed at a low energy, and then fluorine ions are implanted at a comparatively low dose, to form the fluorine implanted layers **109**. The semiconductor substrate **100** is then subjected to the extremely low temperature heat treatment, to recover implantation damage due to the ion implantation. Thereafter, the high-temperature second rapid thermal annealing is performed to activate the boron as impurities for the p-type extension implanted annealed layers **106B**. By following the above process steps, the TED of boron can be suppressed. Since this prevents expansion of the junction in the depth direction, the p-type high-density extension diffused layers **106** having a shallow junction can be formed. In addition, since

diffusion of boron toward the surface of the semiconductor substrate is also suppressed, the boron dose loss is suppressed. For example, the effect of suppressing the boron dose loss can be obtained by setting the fluorine dose at $1 \times 10^{14}/cm^2$ or less.

Thus, by implanting fluorine under the foregoing conditions, it is possible to form, without fail, the low-resistance extension diffused layers **106** in which the junction is shallow, and increase in resistance value due to dose loss is suppressed.

Moreover, the extremely low temperature heat treatment is performed in the fluorine-doped state, and thereafter the high-temperature activation heat treatment is performed. Therefore, damage layers produced due to ion implantation can be recovered as crystal layers, and thus the number of residual defects decreases. As a result, leak current that may occur due to residual defects produced by implantation damage can be prevented.

(Embodiment 3)

Hereinafter, Embodiment 3 will be described with reference to the drawings.

FIGS. **7(a)** to **7(e)** and **8(a)** to **8(d)** are cross-sectional views for illustrating process steps of a fabrication method for a semiconductor device of Embodiment 3 of the present invention.

First, in a process step shown in FIG. **7(a)**, arsenic (As) ions as n-type impurities are implanted in a channel formation region of a semiconductor substrate **100** made of p-type silicon under the conditions of an implantation energy of 140 keV and an implantation dose of $5 \times 10^{12}/cm^2$, to form an n-type channel implanted layer **103A**. Subsequently, phosphorus (P) ions as n-type impurities are implanted in an n-type well formation region of the semiconductor substrate **100** twice, first under the first implantation conditions of an implantation energy of 260 keV and an implantation dose of $4 \times 10^{12}/cm^2$ and then under the second implantation conditions of an implantation energy of 540 keV and an

implantation dose of $1 \times 10^{13}/cm^2$, to form an n-type well implanted layer (not shown) in a portion of the semiconductor substrate **100** under the n-type channel implanted layer **103A**.

In a process step shown in FIG. **7(b)**, immediately after formation of the n-type channel implanted layer **103A** and the n-type well implanted layer, the semiconductor substrate **100** is subjected to first rapid thermal annealing (RTA) in which the temperature of the semiconductor substrate **100** is raised to about 850° C to about 1050° C at a rise rate of about 100° C/s or more, preferably about 200° C/s, and then the peak temperature is held for ten seconds at the longest or is not held at all. With the first rapid thermal annealing, an n-type channel diffused layer **103** is formed in the surface portion of the semiconductor substrate **100**. Simultaneously, an n-type well diffused layer **104** is formed in a portion under the n-type channel diffused layer **103** to be in contact with the n-type channel diffused layer **103**. Note herein that the rapid thermal annealing involving no holding of the peak temperature refers to a kind of heat treatment in which the heat treatment temperature is lowered as soon as it reaches the peak.

In a process step shown in FIG. **7(c)**, a silicon oxide film having a thickness of about 1.5 nm and a polysilicon film having a thickness of about 150 nm are formed in this order over the semiconductor substrate **100**. The silicon oxide film and the polysilicon film are then patterned by photolithography and dry etching, to form a gate insulating film **101** and a gate electrode **102**, respectively. In place of the silicon oxide film, a silicon oxide nitride (SiON) film or a high dielectric insulating film (high-k film) such as a hafnium oxide (HfO_x) film may be used as the gate insulating film. In place of the polysilicon film, a polymetal film may be used as the gate electrode.

In a process step shown in FIG. **7(d)**, boron (B) ions as p-type impurities are implanted in the semiconductor substrate **100** using the gate electrode **102** as a mask under the conditions of an implantation energy of 0.5 keV and an implantation dose of 5 ×

$10^{13}/cm^2$, to form p-type implanted layers **106a**. Subsequently, fluorine ions are implanted in the semiconductor substrate **100** using the gate electrode **102** as a mask under the conditions of an implantation energy of 2 keV and an implantation dose of $1 \times 10^{13}/cm^2$, to form fluorine implanted layers **109**.

In a process step shown in FIG. **7(e)**, the resultant semiconductor substrate **100** is subjected to second rapid thermal annealing in which the temperature of the semiconductor substrate **100** is raised to about 850° C to about 1050° C at a rise rate of about 100° C/s or more, preferably about 200° C/s, then the peak temperature is held for ten seconds at the longest or is not held at all, and the temperature is lowered at a drop rate of about 80° C/s. With the second rapid thermal annealing, the implanted fluorine is diffused toward the surface of the substrate, and p-type diffused layers **106b** having a shallow junction are formed in regions of the semiconductor substrate **100** on both sides of the gate electrode **102**.

In process steps shown in FIGS. **7(d)** and **7(e)**, that is, the ion implantation of boron and fluorine and the second rapid thermal annealing, are taken as one process unit, and this process unit is repeated six times. As a result, p-type extension implanted layers **106A** having a predetermined impurity concentration can be obtained as shown in FIG. **8(a)**. The number of times of repetition of the process unit is not limited to six. However, the process unit must be repeated until the predetermined impurity concentration is obtained, and the ion implantation must be performed at a dose with which no amorphous layer will be formed in the substrate by each time of ion implantation of boron and fluorine. Also, immediately after each of the plurality of times of ion implantation, the high-temperature, short-time rapid thermal annealing must be performed. Hereinafter, the plurality of times, for example, six times of heat treatment are simply called the second heat treatment collectively, for convenience.

In a process step shown in FIG. **8(a)**, after formation of the fluoride implanted layers **109** as a result of the last-time fluorine implantation in the repetition of the process unit, arsenic (As) ions as n-type impurities are implanted in the semiconductor substrate **100** using the gate electrode **102** as a mask under the conditions of an implantation energy of 130 keV and an implantation dose of $4 \times 10^{13}/cm^2$, to form n-type pocket impurity implanted layers **107A**. At this time, p-type extension implanted layers **106A** having a shallow junction are formed by the process units performed six times.

In a process step shown in FIG. **8(b)**, the last-time second rapid thermal annealing in the repetition of the process unit is performed, to form p-type high-density extension diffused layers **106** having a shallow junction, made from diffusion of the boron ions contained in the p-type extension implanted layers **106A** (p-type implanted layer **106a** × 6), in regions of the semiconductor substrate **100** on both sides of the gate electrode **102**. Also formed are n-type pocket diffused layers **107**, made from diffusion of the arsenic ions contained in the n-type pocket implanted layers **107A**, in regions under the extension diffused layers **106** to be in contact with the extension diffused layers **106**.

In a process step shown in FIG. **8(c)**, a silicon nitride film having a thickness of about 50 nm is deposited over the entire top surface of the semiconductor substrate **100** including the gate electrode **102** by CVD, for example. The deposited silicon nitride film is then subjected to anisotropy etching, to form sidewalls **108** made of the silicon nitride film on both walls of the gate electrode **102**. In place of the silicon nitride film, a silicon oxide film or a silicon oxide nitride film may be used as the sidewall **108**. Otherwise, a laminate film composed of at least two films among a silicon nitride film, a silicon oxide film and a silicon oxide nitride film may be used.

In a process step shown in FIG. **8(d)**, boron as p-type impurities are implanted in the semiconductor substrate **100** using the gate electrode **102** and the sidewalls **108** as a

mask under the conditions of an implantation energy of 10 keV and an implantation dose of $3 \times 10^{15}/cm^2$, to form high-density source/drain implanted layers. The resultant semiconductor substrate **100** is subjected to third rapid thermal annealing in which the temperature of the semiconductor substrate **100** is raised to about 850° C to about 1050° C at a rise rate of about 200° C/s to 250° C/s, and then the peak temperature is held for ten seconds at the longest or is not held at all. With the third rapid thermal annealing, p-type high-density source/drain diffused layers **105**, made from diffusion of the boron ions in the high-density source/drain implanted layers, are formed in regions of the semiconductor substrate **100** on both outer sides of the sidewalls **108**. The p-type high-density source/drain diffused layers **105** are connected with the p-type high-density extension diffused layers **106** and have a junction deeper than the extension diffused layers **106**. The junction of the p-type high-density source/drain diffused layers **105** should also be deeper than the junction of the n-type pocket diffused layers **107**. As a result, the p-type high-density extension diffused layers **106** and the n-type pocket diffused layers **107** exist only under the sidewalls **108**.

In the fabrication method for a semiconductor device of Embodiment 3, one process unit composed of the boron implantation, the fluorine implantation and the activation heat treatment is repeated a plurality of times so that the p-type high-density extension diffused layers **106** having a predetermined impurity concentration can be formed. In one time of ion implantation, boron and fluorine are respectively implanted at a dose with which the substrate is kept from becoming amorphous. As a result, it is possible to form, without fail, the low-resistance extension diffused layers **106** in which the junction is shallow and increase in resistance value due to dose loss is suppressed.

As described in Embodiment 1, optimum implantation conditions have been found for suppressing the TED of boron. If the fluorine density is so high that the semiconductor

substrate is made amorphous, the boron junction will become deep and also the boron dose loss will increase. In the case of formation of higher-density boron diffused layers, if boron is implanted at a dose high enough to allow the substrate to become amorphous, it is considered to be difficult to form shallow diffused layers even when fluorine is implanted.

In Embodiment 3, ion implantation of boron and fluorine is performed in a plurality of times, to prevent the substrate from becoming amorphous by the ion implantation. During the second rapid thermal annealing for activation, therefore, boron and fluorine are diffused in the semiconductor substrate that is kept in the crystal state. Accordingly, with the effect of fluorine of suppressing diffusion of boron, the shallow p-type high-density extension diffused layers can be attained. In the case that the boron implantation energy is made lower in an attempt to obtain a shallower junction, the dose with which the semiconductor substrate becomes amorphous also decreases. However, this problem can be avoided by performing the ion implantation in a plurality of times with a low dose, and performing the rapid thermal annealing every time of ion implantation to recover the crystallinity of the semiconductor substrate. This method is also applicable to formation of the high-density source/drain diffused layers **105** by increasing the number of times of performing boron implantation in the formation of the high-density source/drain diffused layers.

In implanting boron and fluorine a plurality of times, rotating implantation in which the angle of the ion implantation, for example, the twist angle is changed for every implantation may be performed.

In Embodiments 1 to 3, arsenic ions were used as the impurity ions for the n-type channel diffused layers **103**. Alternatively, ions of an element that exhibits n-type conductivity and has a mass number greater than arsenic, such as antimony (Sb), may be used, or both ions of such an element and arsenic ions may be used. P-channel MIS

transistors were used to describe the semiconductor device of the present invention. Alternatively, n-channel MIS transistors may be used. In n-channel MIS transistors, n-type impurity ions constituting the extension diffused layers may be arsenic (As) ions or ions of any of group VB elements having a mass number greater than arsenic, such as antimony (Sb) ions and bismuth (Bi) ions.

[Effects of the Invention]

In a semiconductor device and a fabrication method therefore according to the present invention, excessively high-speed diffusion of impurities in extension implanted layers during rapid thermal annealing for activation is suppressed by forming the extension implanted layers and then forming fluorine doped layers. Accordingly, it is possible to provide a semiconductor device including MIS transistors having low-resistance high-density extension diffused layers in which the impurity profile is steep, the junction is shallow, and increase in resistance value due to dose loss is suppressed.

[Brief Description of the Drawing]

[Figure 1] **(a)** to **(d)** are cross-sectional views for illustrating process steps of a fabrication method for a semiconductor device of Embodiment 1 of the present invention.

[Figure 2] **(a)** to **(d)** are cross-sectional views for illustrating process steps of the fabrication method for a semiconductor device of Embodiment 1 of the present invention.

[Figure 3] **(a)** is a graph showing the change of the junction depth of boron with the annealing time.

(b) is a graph showing the change of the density of boron implanted in the semiconductor substrate with the annealing time.

[Figure 4] **(a)** to **(e)** are cross-sectional views for illustrating process steps of a fabrication method for a semiconductor device of Embodiment 2 of the present invention.

[Figure 5] **(a)** to **(d)** are cross-sectional views for illustrating process steps of the

fabrication method for a semiconductor device of Embodiment 2 of the present invention.

[Figure 6] graphs showing impurity profiles in the depth direction from the surface of a substrate in some steps of the fabrication method of Embodiment 2 of the present invention.

(a) is a graph showing the impurity profile observed immediately after ion implantation.

(b) is a graph showing the impurity profile observed immediately after extremely low temperature heat treatment.

(c) is a graph showing the impurity profile observed immediately after activation heat treatment.

[Figure 7] **(a)** to **(e)** are cross-sectional views for illustrating process steps of a fabrication method for a semiconductor device of Embodiment 3 of the present invention.

[Figure 8] **(a)** to **(d)** are cross-sectional views for illustrating process steps of the fabrication method for a semiconductor device of Embodiment 3 of the present invention.

[Figure 9] **(a)** to **(e)** are cross-sectional views for illustrating process steps of a conventional fabrication method for a semiconductor device.

[Description of the Reference Numerals]

100 p-type semiconductor substrate

101 gate insulating film

102 gate electrode

103 n-type channel diffused layer

103A n-type channel implanted layer

104 n-type well diffused layer

105 p-type high-density source/drain diffused layer

106 p-type high-density extension diffused layer

106A p-type extension implanted layer

106B p-type extension implanted annealed layer

106a p-type implanted layer

106b p-type diffused layer

107 n-type pocket diffused layer

107A n-type pocket impurity implanted layer

107B n-type pocket implanted annealed layer

108 sidewall

109 fluorine implanted layer

109B fluorine implanted annealed layer

[Name of the Document] Abstract

[Abstract]

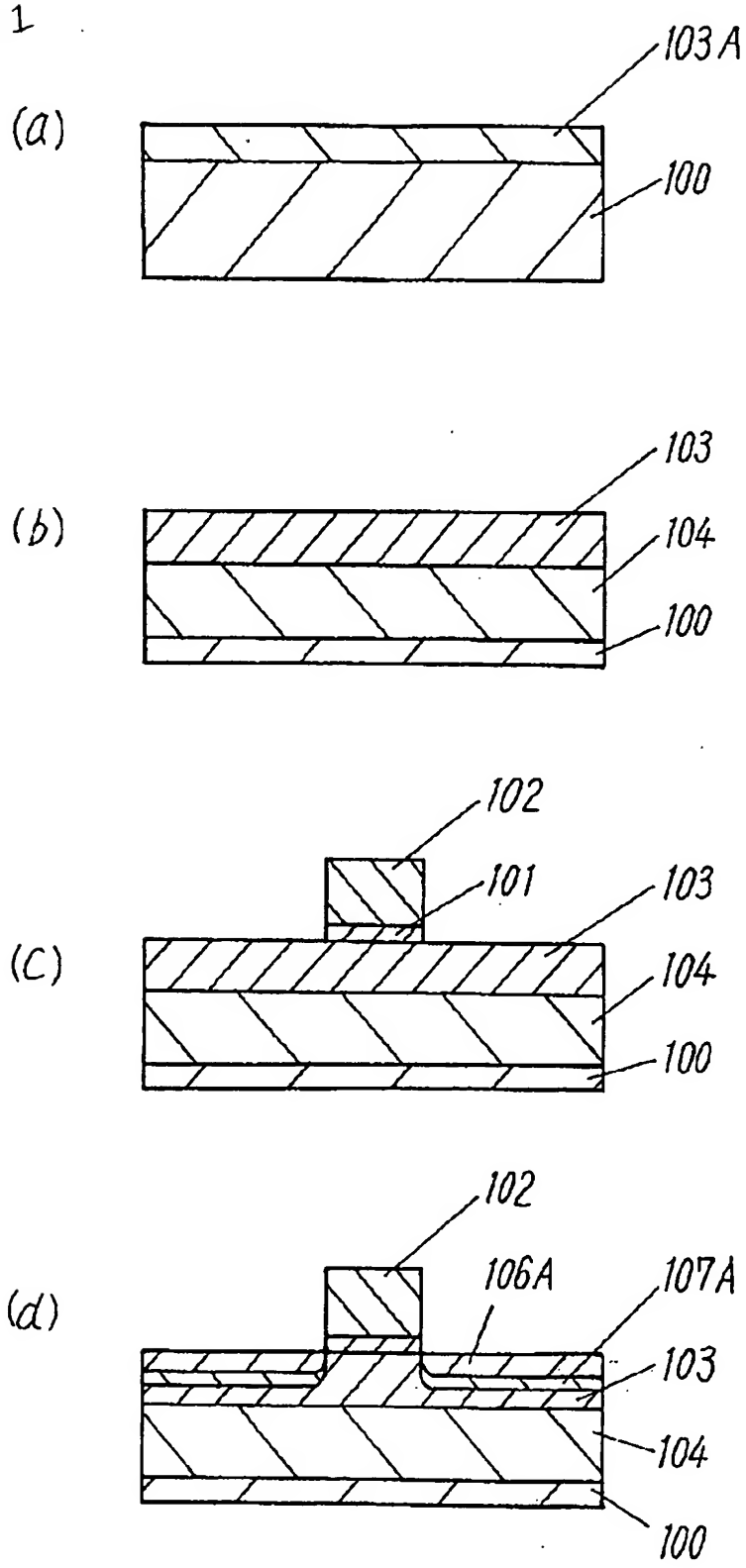
[Purpose] An object of the present invention is to provide a semiconductor device in which the junction of high-density extension diffused layers is shallow and the resistance is reduced, and a method for fabricating such a semiconductor device.

[Solution] An n-type channel diffused layer **103** and an n-type well diffused layer **104** are formed in a semiconductor substrate **100**. Then, a gate insulating film **101** and a gate electrode **102** are formed on the semiconductor substrate **100**. Using the gate electrode **102** as a mask, boron and arsenic are implanted to form p-type extension implanted layers **106A** and n-type pocket impurity implanted layers **107A**. Fluorine is then implanted using the gate electrode **102** as a mask to form fluorine implanted layers **109**. The resultant semiconductor substrate **100** is subjected to rapid thermal annealing, forming p-type high-density extension diffused layers **106** and n-type pocket diffused layers **107**. Sidewalls **108** and p-type high-density source/drain diffused layers **105** are then formed.

[Selected Figure] Figure **1**

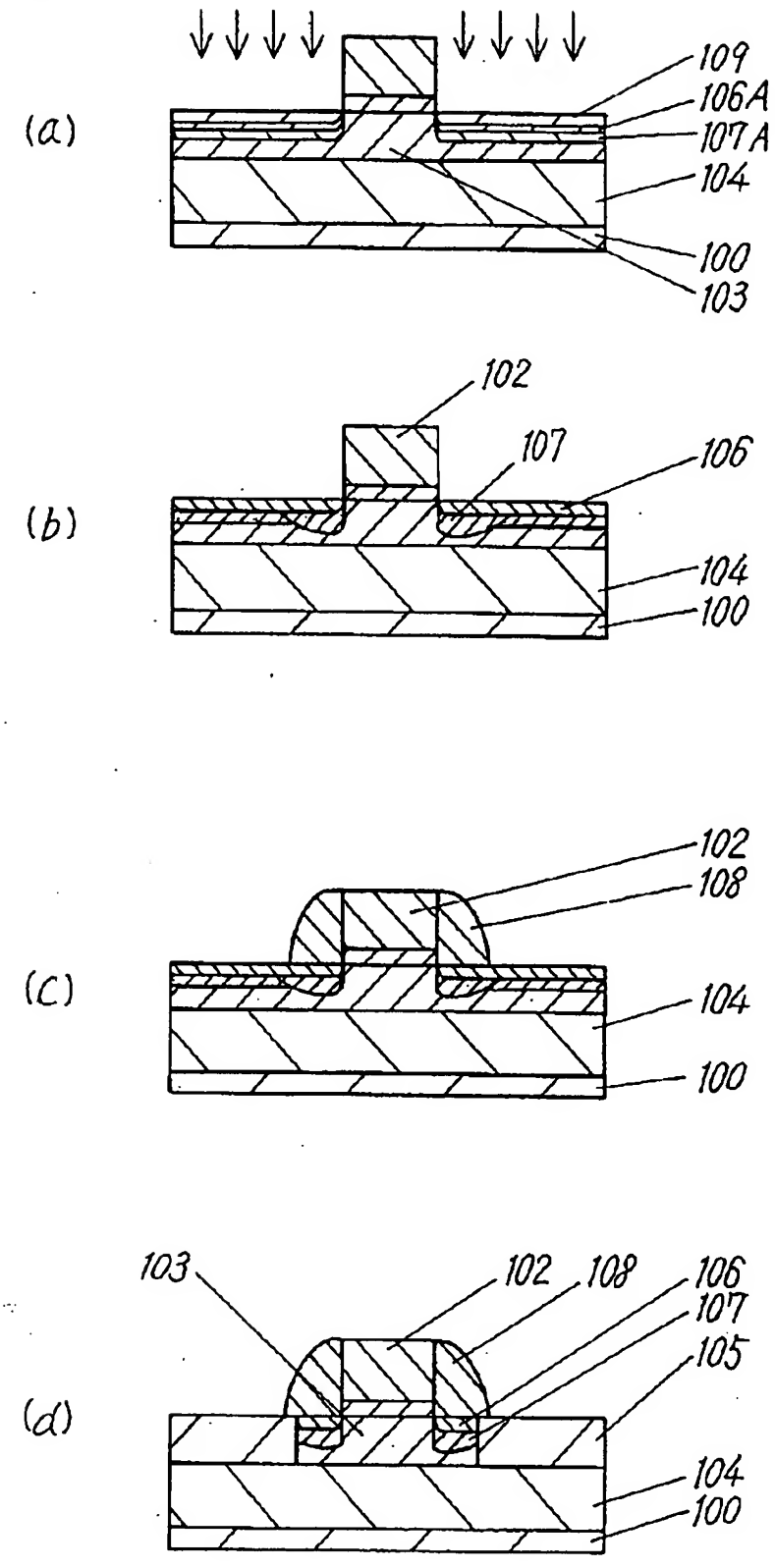
【図1】

Figure 1


(a)
103A
100
(b)
103
104
100
(C)
102
101
103
104
100
(d)
102
106A
107A
103
104
100

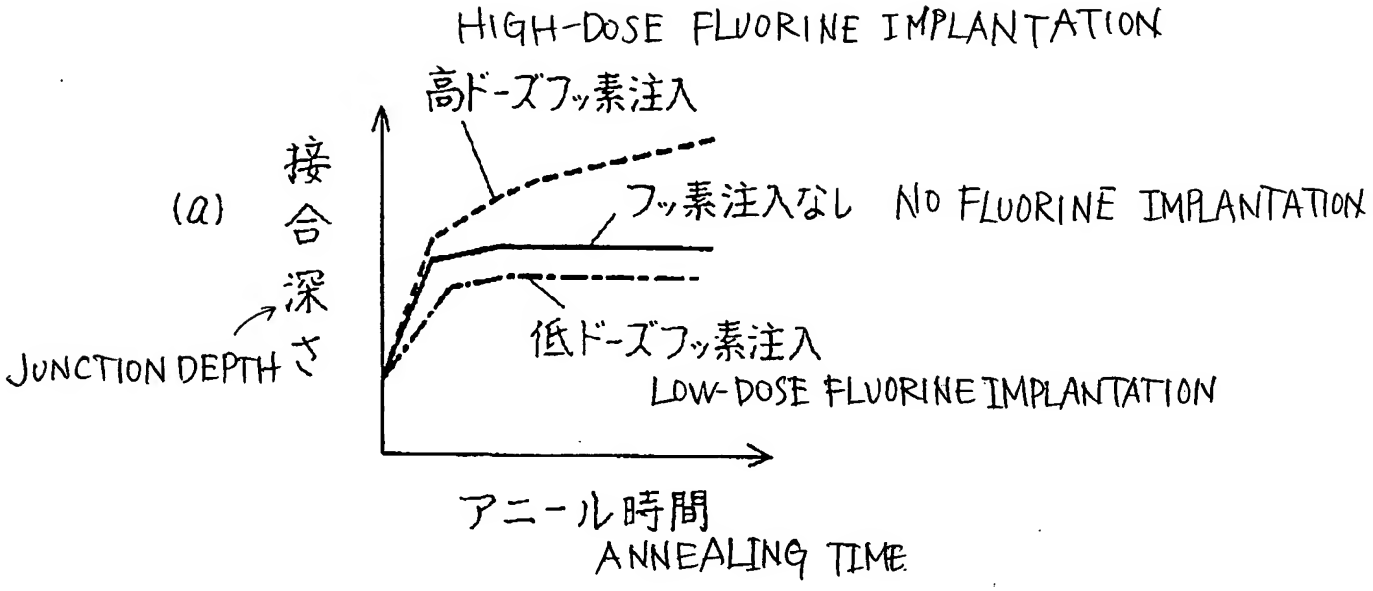
【図2】

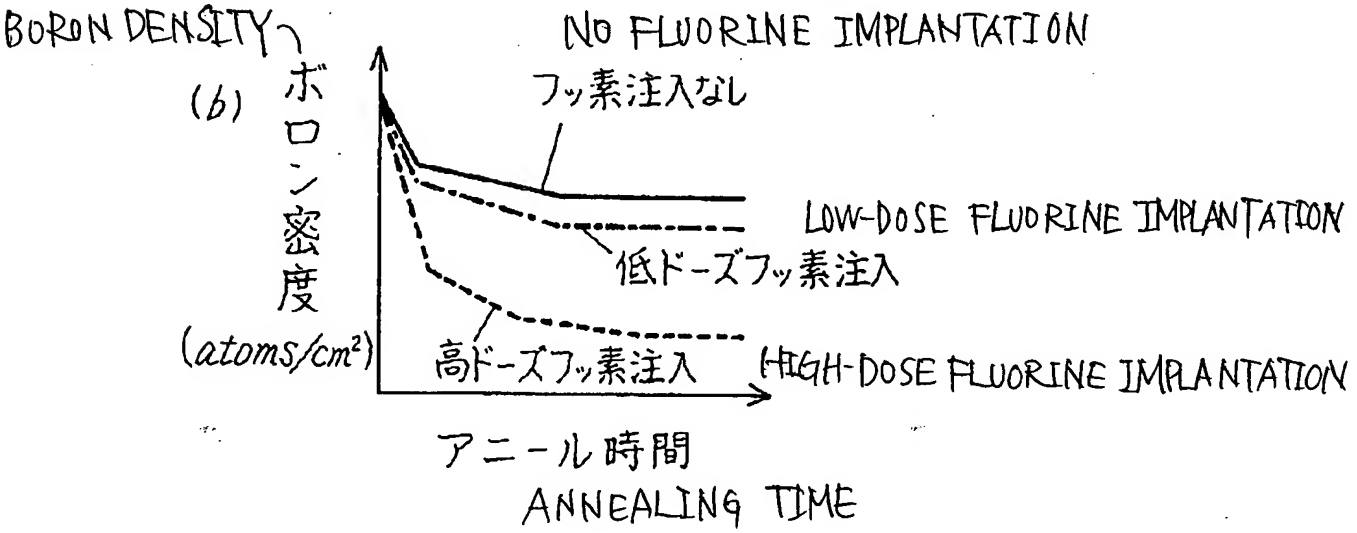
Figure 2


(a)
109
106A
107A
104
100
103
(b)
102
107
106
104
100
(c)
102
108
104
100
(d)
103
102
108
106
107
105
104
100

【図3】

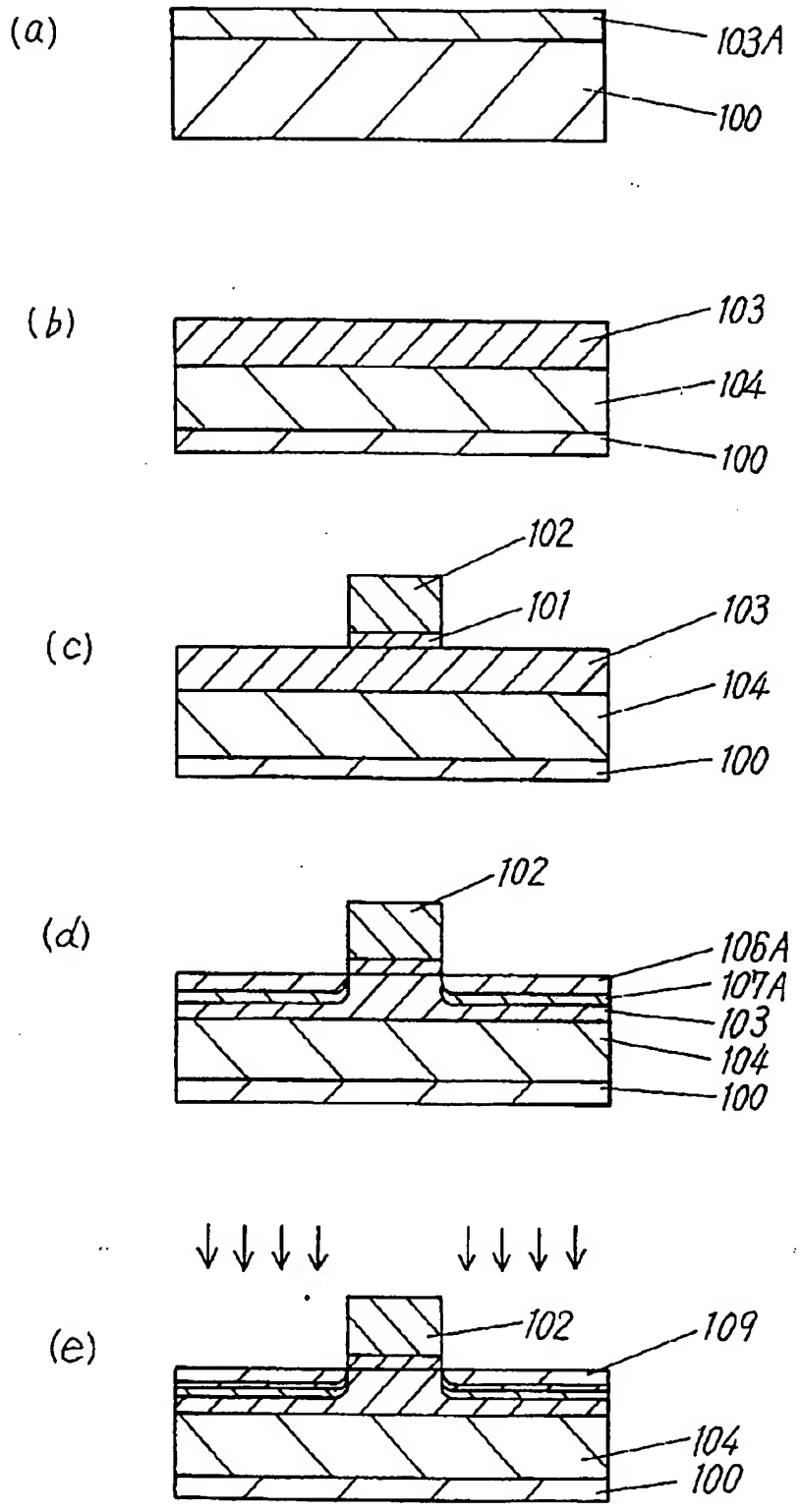
Figure 3


HIGH-DOSE FLUORINE IMPLANTATION
高ドーズフッ素注入
(a)
接合深さ
JUNCTION DEPTH
フッ素注入なし
NO FLUORINE IMPLANTATION
低ドーズフッ素注入
LOW-DOSE FLUORINE IMPLANTATION
アニール時間
ANNEALING TIME


BORON DENSITY
(b)
ボロン密度
(atoms/cm²)
NO FLUORINE IMPLANTATION
フッ素注入なし
LOW-DOSE FLUORINE IMPLANTATION
低ドーズフッ素注入
高ドーズフッ素注入
HIGH-DOSE FLUORINE IMPLANTATION
アニール時間
ANNEALING TIME

【図4】

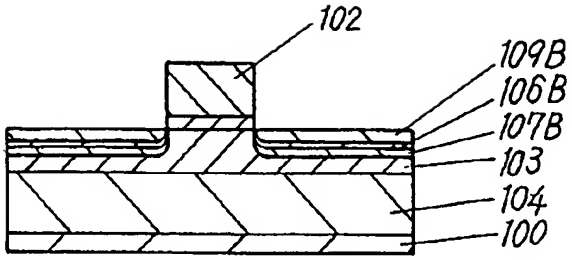
FIGURE 4


(a)
103A
100
(b)
103
104
100
(c)
102
101
103
104
100
(d)
102
106A
107A
103
104
100
(e)
102
109
104
100

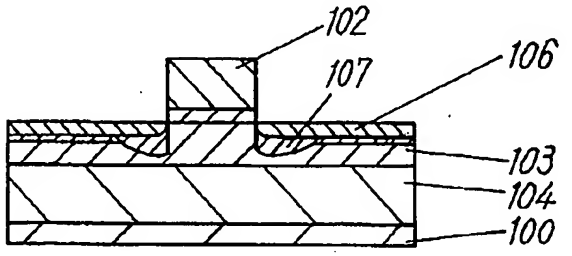
【図5】

FIGURE 5

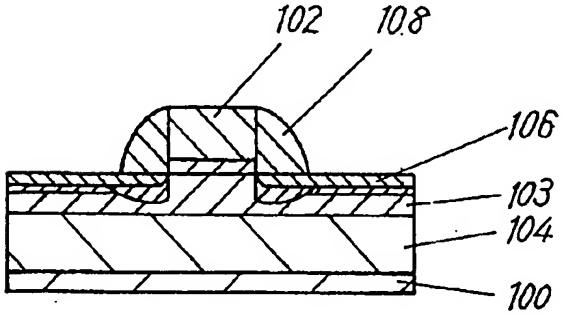
(a)



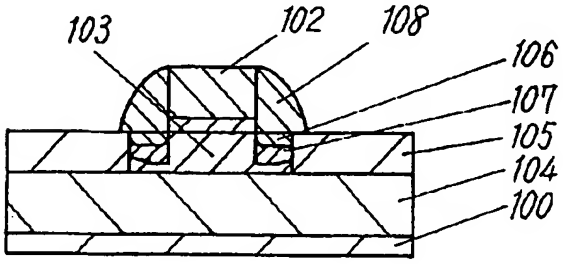
(b)



(c)

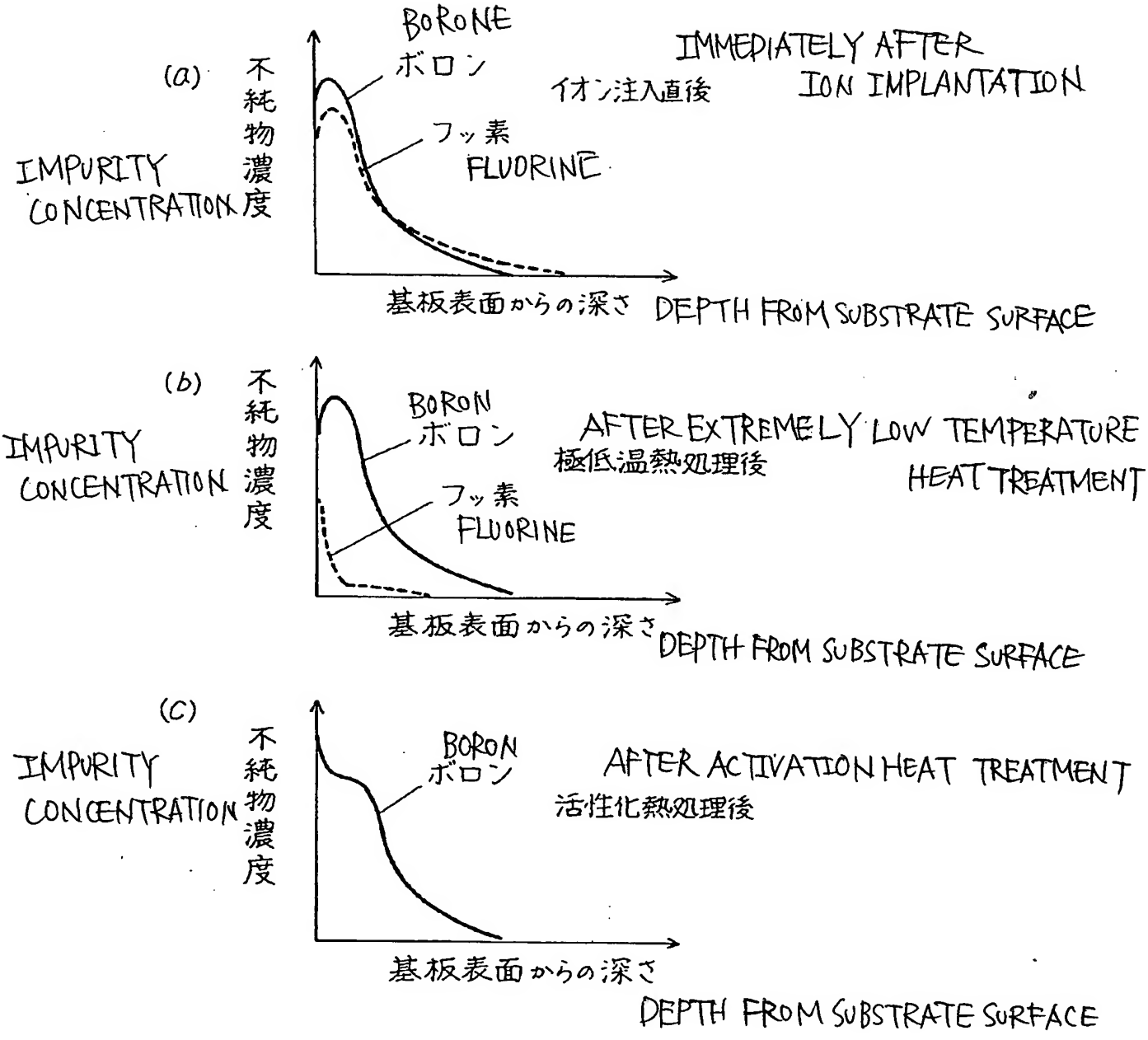


(d)



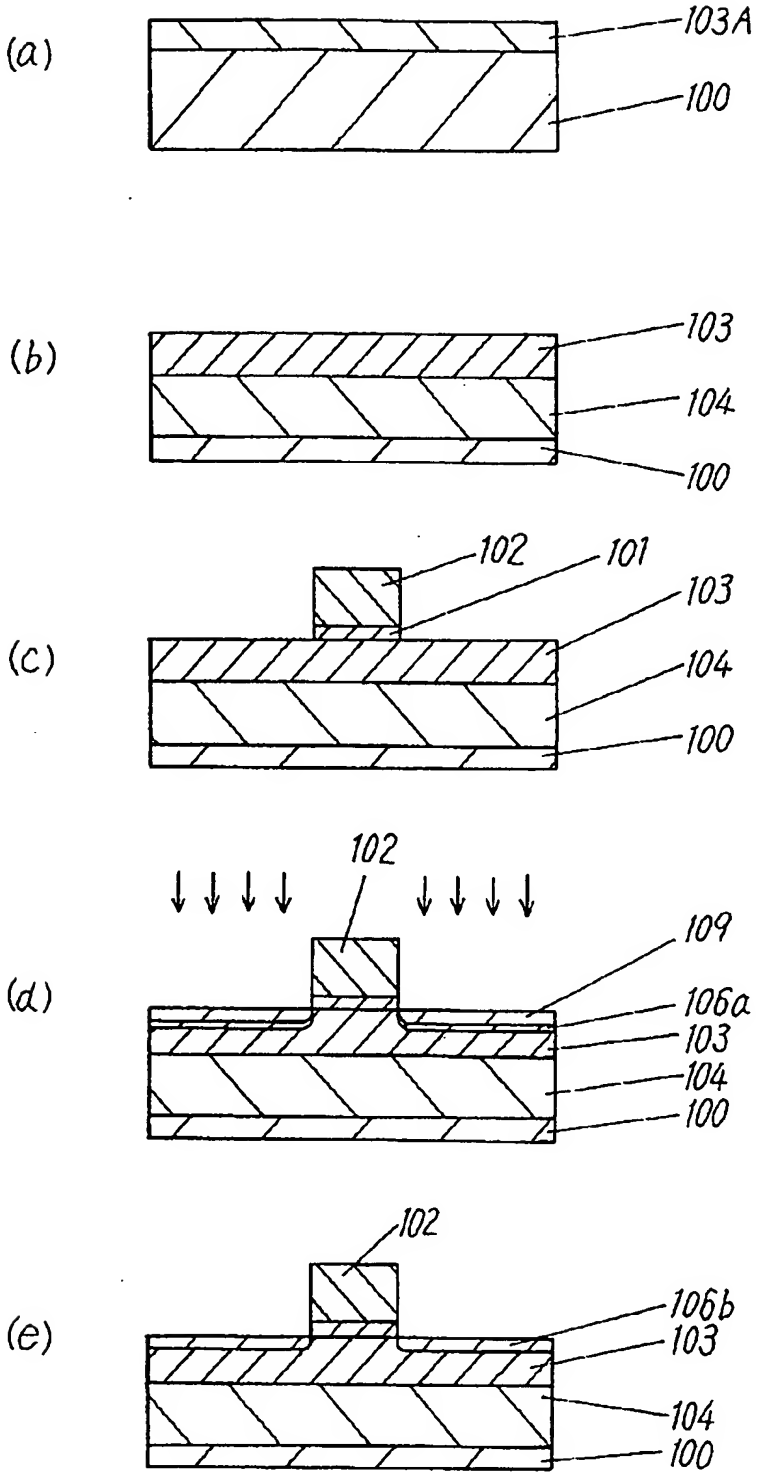
【図6】

FIGURE 6


(a)
不純物濃度
IMPURITY CONCENTRATION
BORONE
ボロン
フッ素
FLUORINE
IMMEDIATELY AFTER ION IMPLANTATION
イオン注入直後
基板表面からの深さ DEPTH FROM SUBSTRATE SURFACE
(b)
不純物濃度
IMPURITY CONCENTRATION
BORON
ボロン
フッ素
FLUORINE
AFTER EXTREMELY LOW TEMPERATURE HEAT TREATMENT
極低温熱処理後
基板表面からの深さ DEPTH FROM SUBSTRATE SURFACE
(C)
不純物濃度
IMPURITY CONCENTRATION
BORON
ボロン
AFTER ACTIVATION HEAT TREATMENT
活性化熱処理後
基板表面からの深さ
DEPTH FROM SUBSTRATE SURFACE

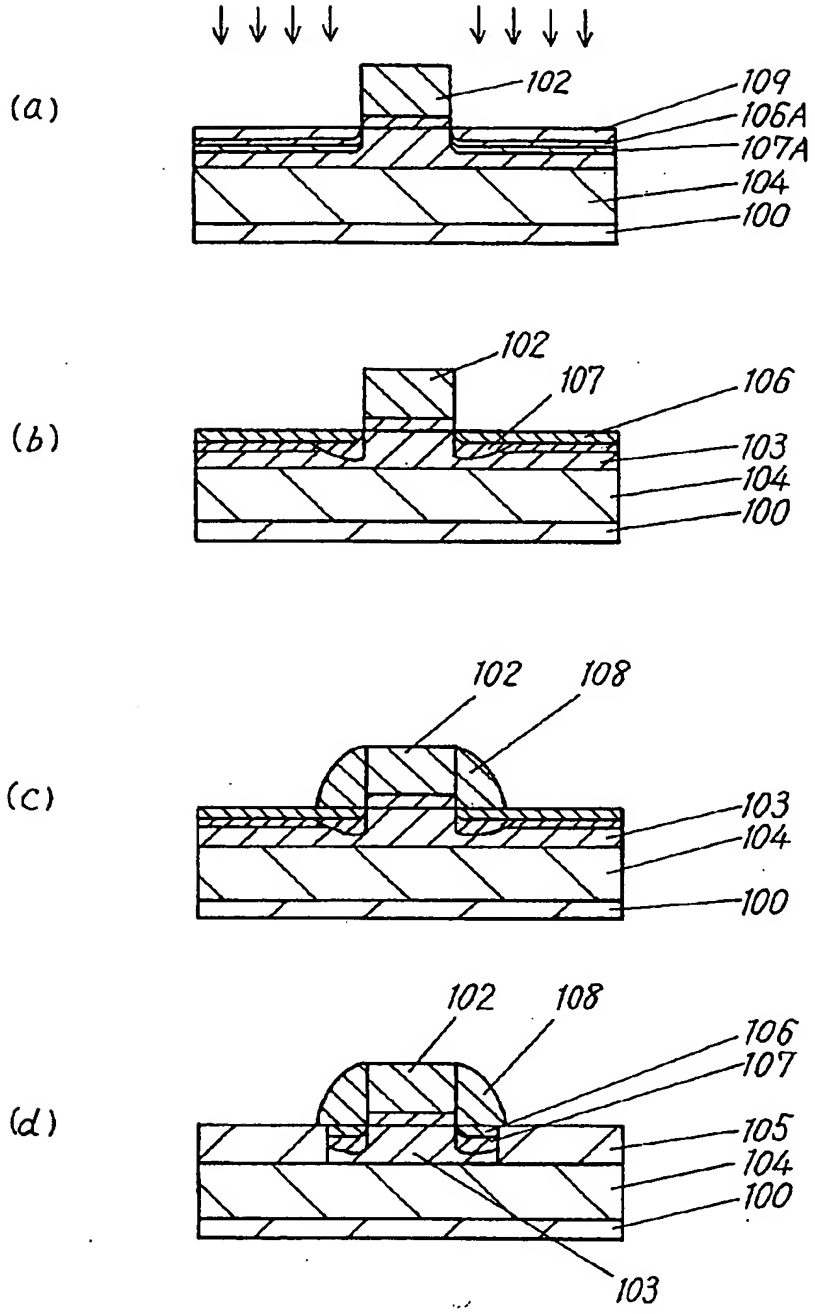
【図7】

FIGURE 7


(a)
103A
100
(b)
103
104
100
(c)
102
101
103
104
100
(d)
102
109
106a
103
104
100
(e)
102
106b
103
104
100

【図8】

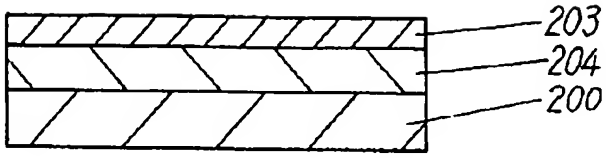
FIGURE 8


(a)
102
109
106A
107A
104
100
(b)
102
107
106
103
104
100
(c)
102
108
103
104
100
(d)
102
108
106
107
105
104
100
103

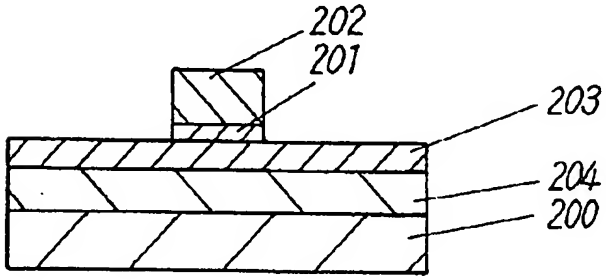
【図9】

FIGURE 9

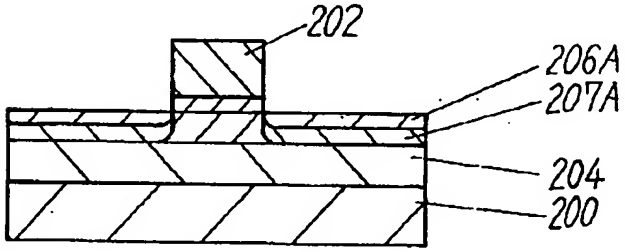
(a)



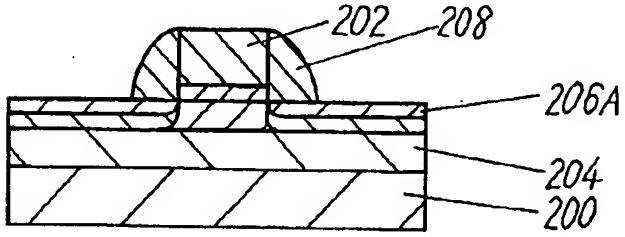
(b)



(c)



(d)



(e)